TOSHIBA

INTEGRATED CIRCUIT TECHNICAL DATA

MICROCOMPUTER

LSI DATA BOOK

July 1984

TOSHIBA CORPORATION

TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT

TMP8049P/8049P-6/8049PI-6

TMP8039P/8039P-6/8039PI-6

N-CHANNEL SILICON GATE MOS

8-BIT SINGLE-CHIP MICROCOMPUTER

GENERAL DESCRIPTION

The TMP8049P, from here on referred to as the TMP8049, is a single chip microcomputer fabricated in N-channel Silicon Gate MOS technology which provides internal 8-bit parallel architecture.

The following basic architectural functions of a computer have been included in a single chip; an 8-bit CPU, 128 × 8 RAM data memory, 2K × 8 ROM program memory, 27 I/O lines and an 8-bit timer/event counter.

The TMP8049 is particularly efficient as a controller. It has extensive bit handling capability as well as facilities for both binary and BCD arithmetic.

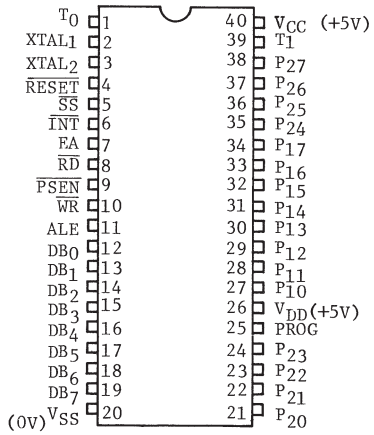
The TMP8039P is the equivalent of a TMP8049 without ROM program memory on chip. By using this device with external EPROM or RAM, software debugging becomes easy.

The TMP8049P-6/TMP8039P-6 is a lower speed (6MHz) version of the TMP8049P/TMP8039P.

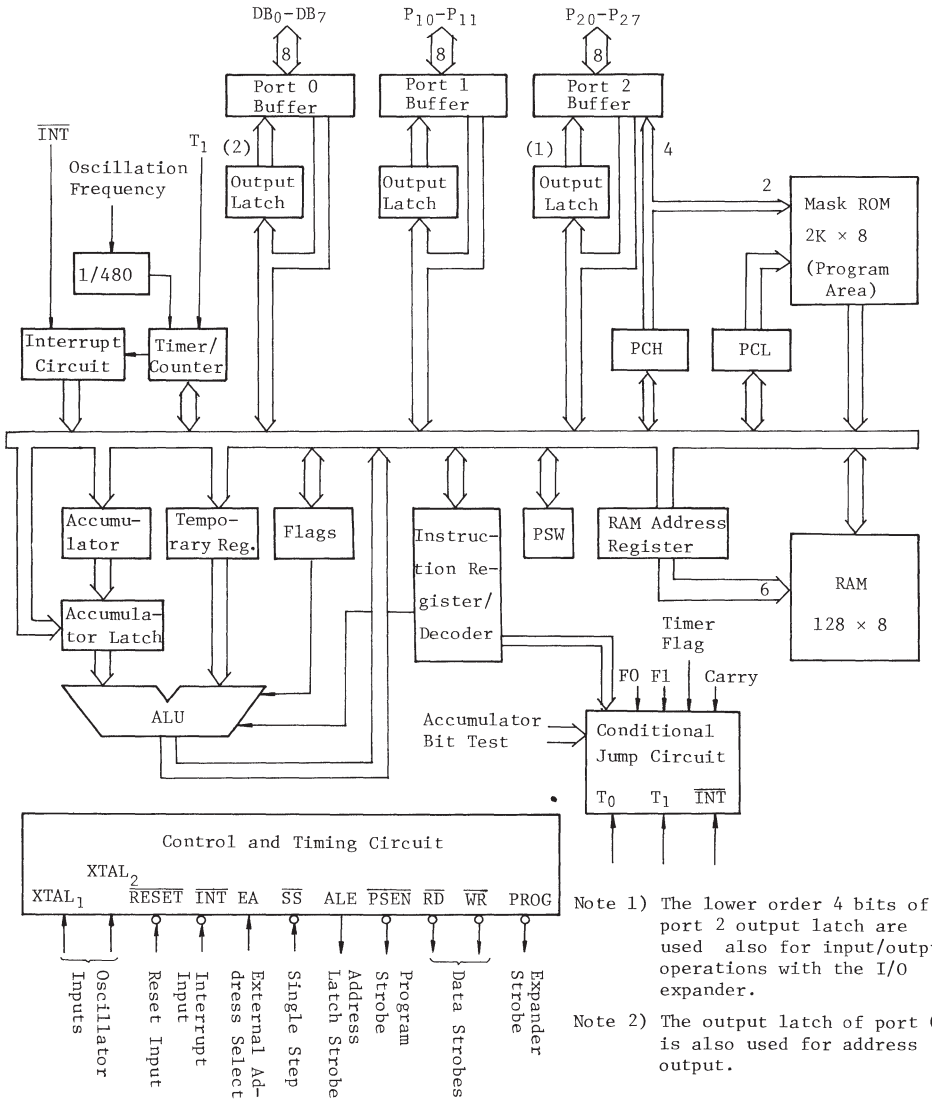
FEATURES

- Compatible with Intel's 8049
- 1.36μS Instruction Cycle
- All instruction 1 or 2 cycles
- Over 90 instructions; 70% single byte
- Easy expandable memory and I/O
- 2K × 8 masked ROM
- 128 × 8 RAM
- 27 I/O lines
- Interval Timer/Event Counter
- Single level interrupt
- Single 5V supply
- -40°C to +85°C Operation (TMP8049PI-6/ TMP8039PI-6 : Industrial Specification)

PIN CONNECTIONS (Top View)



BLOCK DIAGRAM



Note 1) The lower order 4 bits of port 2 output latch are used also for input/output operations with the I/O expander.

Note 2) The output latch of port 0 is also used for address output.

PIN NAMES AND PIN DESCRIPTION

V_{SS} (Power Supply)

Circuit GND potential

V_{DD} (Power Supply)

+5V during operation Low power standby pin for TMP8049 RAM

V_{CC} (Main Power Supply)

+5V during operation

PROG (Output)

Output strobe for the TMP8243P I/O expander

P_{10}-P_{17} (Input/Output) Port 1

8-bit quasi-bidirectional port (Internal Pullup $\cong$ 50KΩ).

P_{20}-P_{27} (Input/Output) Port 2

8-bit quasi-bidirectional port (Internal Pullup $\cong$ 50KΩ).

P_{20}-P_{23} Contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for the TMP8243P.

DB_0 -DB_7 (Input/Output, 3 State)

Ture bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.

T_0 (Input/Output)

Input pin testable using the conditional transfer instructions JTO and JNTO. T_0 can be designated as a clock output using ENTO CLK instruction.

T_1 (Input)

Input pin testable using the JT1 and JNT1 instruction. Can be designated the event counter input using the timer/STRT CNT instruction.

$\overline{INT}$ (Input)

External interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active Low)

$\overline{RD}$ (Output)

Output strobe activated during a Bus read. Can be used to enable data onto the Bus from an external device. Used as a Read Strobe to External Data Memory (Active Low).

$\overline{WR}$ (Output)

Output strobe during a Bus write (Active Low) Used as a Write Strobe to External Data Memory.

RESET (Input)

Active Low signal which is used to initialize the Processor. Also used during Power down.

ALE (Output)

Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.

$\overline{\text{PSEN}}$ (Output)

Program Store Enable. This output occurs only during a fetch to external program memory (Active Low).

$\overline{\text{SS}}$ (Input)

Single step input can be used in conjunction with ALE to "single step" processor through each instruction when $\overline{\text{SS}}$ is low the CPU is placed into a wait state after it has completed the instruction being executed.

EA (Input)

External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug and essential for testing and program verification. (Active High).

XTAL 1 (Input)

One side of crystal input for internal oscillator. Also input for external source.

XTAL 2 (Input)

Other side of crystal input.

FUNCTIONAL DESCRIPTION

1. System Configuration

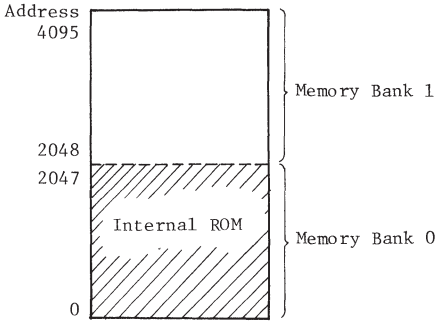
The following system functions of the TMP8049 are described in detail.

(1) Program Memory
(2) Data Memory
(3) I/O Port
(4) Timer/Counter
(5) Interrupt Control Circuit
(6) Stack (Stack Pointer)
(7) Flag 0, Flag 1
(8) Program Status Word (PSW)
(9) Reset
(10) Oscillator Circuit

(1) Program Memory

- The maximum memory that can be directly addressed by the TMP8049 is 4096 bytes. The first 2048 bytes from location 0 through 2047 can be internal resident mask ROM. The rest of the 2048 bytes of addressable memory are external to the chip. The TMP8039 has no internal resident memory; all memory must be external.

There are three locations in Program Memory of special importance.



Program Memory Area

- Location 0

  Activating the Reset line of the processor causes the first instruction to be fetched from Location 0.

- Location 3

  Activating the interrupt line of the processor (if interrupt enabled) causes a jump to subroutine defined by address held in Location 3.

- Location 7

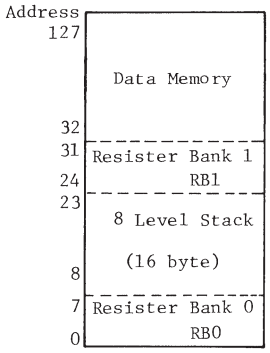
  A timer/counter interrupt resulting from a timer/counter overflow (if enabled) causes a jump to a subroutine defined by address held in Location 7.

- Program addresses 0-2047 and 2048-4095 are called memory banks 0 and 1 respectively. Switching of memory banks is achieved by changing the most significant bit of the program counter (PC) during execution of an unconditional jump instruction or call instruction executed after using SEL MB0 or SEL MB1.

  Reset operation automatically selects Bank 0.

(2) Data Memory

- Resident Data Memory (volatile RAM) is organized as 128 words by 8-bits wide.
- The first 8 locations (0 - 7) of the memory array are designated as working registers and are directly addressable by several instructions.
  By executing a Register Bank switch instruction (SEL RB1) locations 24 - 31 are designated as the working registers in place of 0 - 7.



Internal Data Memory Area

- RAM locations 8 - 23 serve a dual role in that they contain the program counter stack which is a stack 2 bytes wide by 8 levels deep. These locations store returning addresses from subroutines. If the level of subroutine nesting is less than the permitted 8, you free up 2 bytes of RAM for general use for every level of nesting not utilized.
- ALL 128 locations are indirectly addressable through either of two RAM Pointer Registers which reside at R0 and R1 of the Register array.
- The TMP8049 architecture allows extension of the Data Memory to 256 words.

(3) Input/Output Ports

- The TMP8049 has 27 I/O lines which can be used for either input or output. These I/O lines are grouped into 3 ports each having 8 bidirectional lines and 3 "test" inputs which can alter program sequences when tested by conditional jump instructions.
- Ports 1 and 2 are each 8-bits wide and have identical characteristics. Data written to these ports is statically latched and remains unchanged until rewritten. As input ports these lines are non-latching, i.e., inputs must be present until read by an input instruction.
- All lines of Ports 1 and 2 are called quasi-bidirectional because of a special output circuit structure (illustrated in Figure 1). Each line is continously pulled to a +5V level through a high impedance resistive device (50KΩ) which is sufficient to provide the source current for a TTL high level yet can be pulled low by a standard TTL gate thus allowing the same pin to be used for both input and output. In order to speed up the "0" to "1" transition a low impedance device (5KΩ) is switched in momentarily whenever a "1" is written to line. When a "0" is written to line a low impedance device overcomes the pullup and provides TTL current sinking capability.

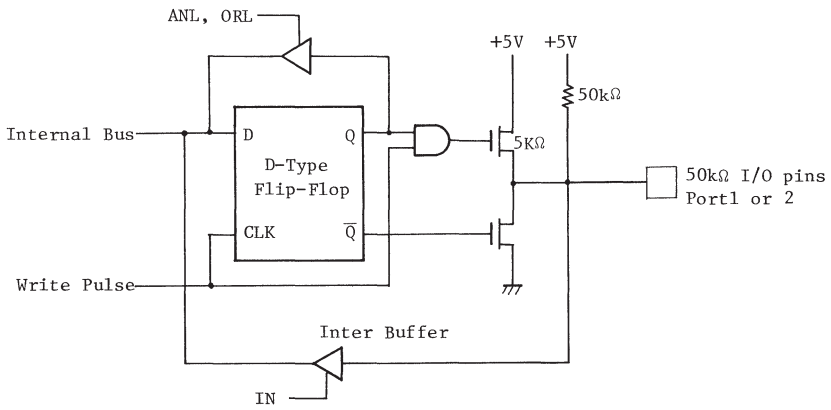


Fig.1 Input/Output Circuit of Port 1, Port 2

- Reset initializes all lines to a high impedance "1" state.
- When external data memory area is not addressed during execution of an internal program, Port 0 (DB0 - DB7) becomes a true bidirectional port (bus) with associated input and output strobes. If bidirectional feature not needed Bus can serve as either a statically latched output port or a non-latched input port. However, I/O lines of this port cannot be intermixed.
- As a static port data is written and latched using the OUTL instruction and inputted using the INS instruction these two commands generate pulses on the corresponding $\overline{RD}$ and $\overline{WR}$ strobe lines.
- As a bidirectional port the MOVX instructions are used to read and write the port which generate the $\overline{WR}$ $\overline{RD}$ strobes.
- When not being written or read, the Bus lines are in a high impedance state.

(4) Timer/Event Counter

- The 8-bit binary up counter can use either of the following frequency inputs

(1) Internal clock (1/480 of OSC frequency)

..... Timer mode

(2) External input clock form T1 terminal

(minimum cycle time 3 × ALE cycle)

..... Event Counter mode

The counter is presettable and readable with two MOV instructions which transfer the content of the accumulator to the counter and vice versa. The counter content is not affected by a Reset and is initialized solely by the MOVT, A instruction. The counter is stopped by a Reset or STOP TCNT instruction and remains stopped until started by START T instruction or as an event counter by a START CNT. Once started the counter will increment to its maximum count (FF) and overflow to Zero continuing its count until stopped by a STOP TCNT instruction or RESET.

The increment from maximum count to Zero (overflow) results in the setting of an overflow flag and the generation of an interrupt request. When interrupt acknowledged a subroutine call to Location 7 will be initiated. Location 7 should store the starting address of the timer or counter service routine. The state of the overflow flag is testable with the conditional JUMP (JTF). The flag is reset by executing a JTF or by RESET. Figure 2 illustrates the concept of the timer circuit.

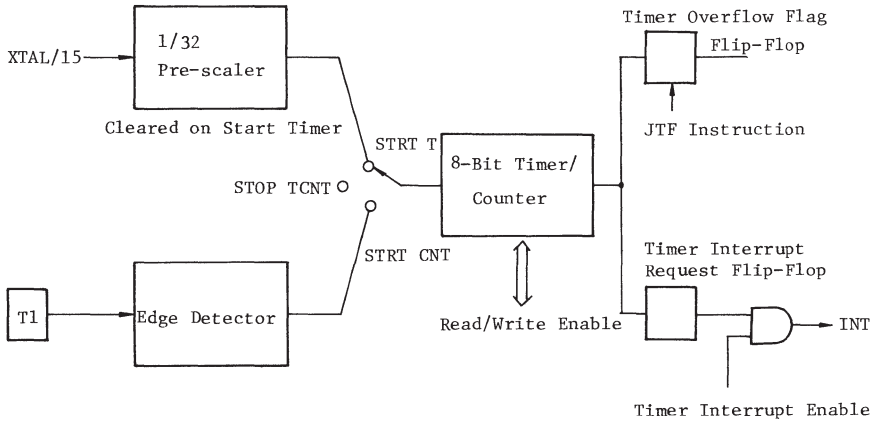


Fig.2 Concept of Timer Circuit

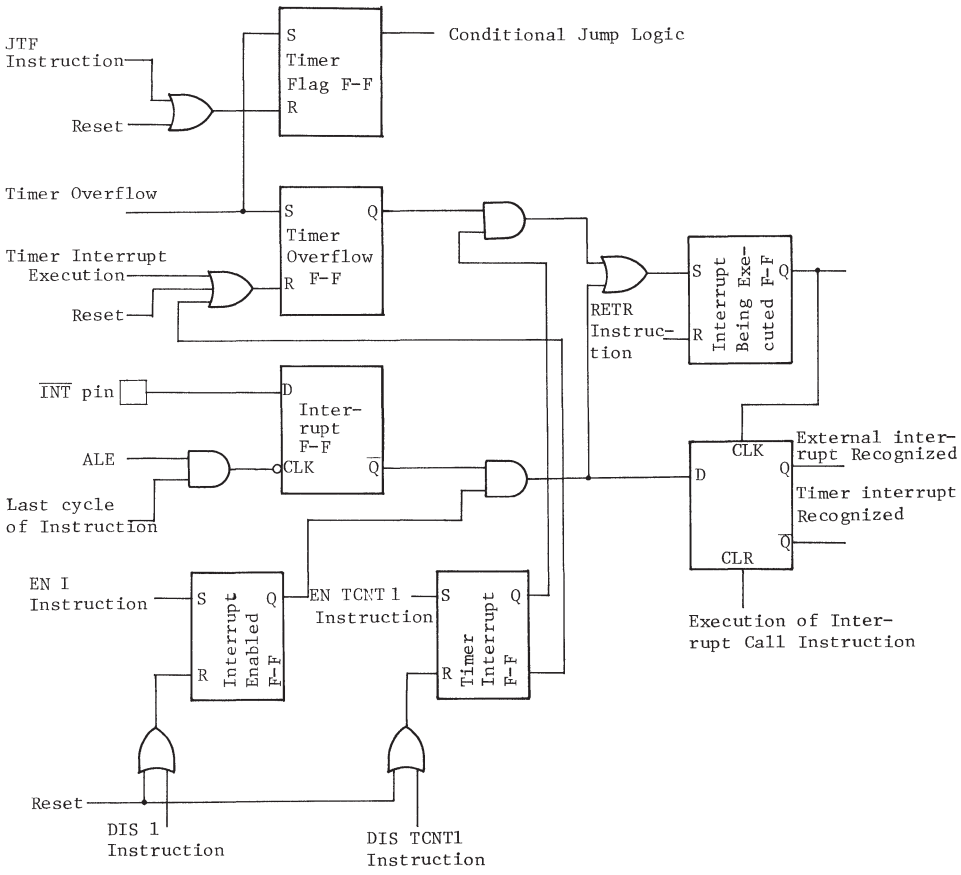


Fig.3 Concept of Interrupt Control Circuit

(5) Interrupt Control Circuit

. There are two distinct types of Interrupts in the TMP8049.

(1) External Interrupt from the $\overline{\text{INT}}$ terminal

(2) Timer Interrupt caused by timer overflow

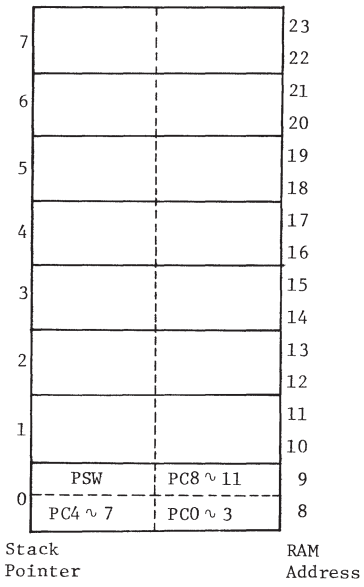
The interrupt system is single level in that once an interrupt is detected all further interrupt requests are ignored until execution of an RETR (which should occur at the end of an interrupt service routine) reenables the interrupt input logic.

- An interrupt sequence is initiated by applying a low level "0" to the $\overline{INT}$ pin. $\overline{INT}$ is level triggered and active low which allows "Wire Oring" of several interrupt sources. The interrupt level is sampled every machine cycle during ALE and when detected causes a "jump to subroutine" at Location 3. As in any call to subroutine, the Program Counter and Program Status Word are saved in the stack.
- When an overflow occurs in the internal timer/event counter an interrupt request is generated which is reserviced as outlined in previous paragraph except that a jump to Location 7 is used instead of 3. If $\overline{INT}$ and times overflow occur simultaneously then external request $\overline{INT}$ takes precedence.
- If an extra external interrupt is needed in addition to $\overline{INT}$ this can be achieved by enabling the counter interrupt, loading FFH in the counter (one less than the terminal count), and enabling the event counter mode. A "1" to "0" transition on T1 will cause an interrupt vector to Location 7.
- The interrupt service routine pointed to be addresses in Location 3 or 7 must reside in memory between 0 and 2047, i,e., Bank 0.

Figure 3 illustrates the concept of the interrupt control circuit.

(6) Stack (stack Pointer)

- An interrupt or Call to a subroutine causes the contents of the program counter to be stored in one of the 8 register pairs of the Program Counter Stack. The pair to be used is determined by a 3-bit stack pointer which is part of the Program Status Word (PSW explained in section (8)). Data RAM locations, 8 through 23 are available as stack registers and are used to store the program counter and 4-bits of PSW as shown in the figure.
- The stack pointer when initialized points to RAM locations 8 and 9. The first subroutine jump or interrupt results in the program counter contents being transferred to Locations 8 and 9. Then the stack pointer is incremented by one to point to Locations 10 and 11. Eight levels of subroutine are obviously possible.
- At the end of a subroutine signalled by a RET or RETR causes the stack pointer to be decremented by one and the contents of the resulting pair to be transferred to the Program Counter.

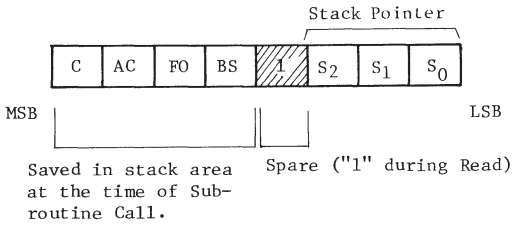


(7) Flag 0, Flag 1, (F0, F1)

- The TMP8049 has two flags F0 and F1 which are used for conditional jump. These flags can be set, reset and tested with the conditional jump instruction JF0.
- F0 is a part of the program status word (PSW) and is saved in the stack area when a subroutine is called.

(8) Program Status Word (PSW)

- An 8-bit status word which can be loaded to and from the accumulator exsists called the Program Status Word (PSW). The PSW is read by a MOV A, PSW and written to by a MOV PSW, A. The information available in the PSW is shown in the diagram below.



Bits 0 - 2 : Stack Pointer Bits(S_0, S_1, S_2)

Bit 3 : Not used ("1" level when read.)

Bit 4 : Working Register Bank Switch Bit (BS)

0 = Bank 0

1 = Bank 1

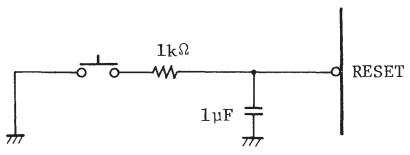
Bit 5 : Flag 0 (FO)

Bit 6 : Auxiliary Carry (AC) carry bit generated by an ADD instruction and used by the decimal adjust instruction DA, A (AC)

Bit 7 : Carry (C) flag which indicates that the previous operation has resulted in the accumulator. (C)

(9) Reset

- The reset input provides a means for initialization of the processor. This Schmitt trigger input has an internal pullup resistor which in combination with an external 1μF capacitor provides an internal reset pulse sufficient length to guarantee that all internal logic is initialized.



If the pulse is generated externally the reset pin must be held at ground (≤0.5V) for at least 50mS after the power supply is within tolerance.

Reset performs the following functions within the chip:

(i) Sets PC to Zero.

(ii) Sets Stack Pointer to Zero.

(iii) Selects Register Bank 0.

(iv) Selects Memory Bank 0.

(v) Sets BUS (DB0 - DB7) to high impedance state. (Except when EA = 5V)

(vi) Sets Ports 1 and 2 to input mode.

(vii) Disables interrupts (timer and external).

(viii) Stops Timer.

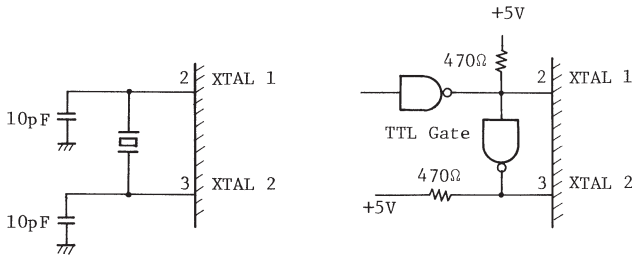
(ix) Clears Timer Flag.

(x) Clears F0 and F1.

(xi) Disables clock output T0.

(10) Oscillator Circuit

- TMP8049 can be operated by the external clock input in addition to crystal oscillator as shown below.



2. Basic Operation and Timing

The following basic operations and timing are explained

(1) Instruction Cycle

(2) External Memory Access Timing

(3) Interface with I/O Expander TMP8243P

(4) Internal Program Verify (Read) Timing

(5) Single Step Operation Timing

(6) Low Power Stand-by Mode

(1) Instruction Cycle

- The instructions of TMP8049 are executed in one or two machine cycles, and one machine cycle consists of five states.
- Fig.4 illustrates its relationship with the clock input to CPU.
- $\phi 2$ clock shown in Fig.4 is derived to outside by ENTO CLK instruction.
- ALE can be also used as the clock to indicate the machine cycle as well as giving the external address latch timing.

(2) External Memory Access Timing

(i) Program Memory Access

- TMP8049 programs are executed in the following three modes.

  (1) Execution of internal program only.

  (2) Execution of both external and internal programs.

  (3) Execution of external program only.

  The external program memory is accessed (instructions are fetched) automatically when the internal ROM address is exceeded in mode (2) and from initial start address 0 in mode (3).

- In the external program memory access operation, the following will occur

  - The contents of the 12-bit program counter will be output on BUS(DB0 - DB7) and the lower 4-bits of Port 2.
  - Address Latch Enable (ALE) will indicate the time at which address is valid. The trailing edge of ALE is used to latch the address externally.
  - Program Store Enable (PSEN) indicates that an external instruction fetch is in progress and serves to enable the external memory device.
  - BUS (DB0 - DB7) reverts to Input mode and the processor accepts its 8-bit contents as an Instruction Word.

- Figure 5 illustrates the timing.

(ii) Access of External Data Memory

- In the extended data memory access operation during READ/WRITE cycle the following occurs

  - The contents of R0 R1 is output onto BUS (DB0 - DB7).
  - ALE indciates address is valid. The trailing edge of ALE is used to latch the address externally.
  - A read $\overline{RD}$ or write $\overline{WR}$ pulse on the corresponding output pins indicates the type of data memory access in progress. Output data valid at trailing edge of $\overline{WR}$ and input data must be valid at trailing edge of $\overline{RD}$.
  - Data (8-bits) is transferred over BUS.

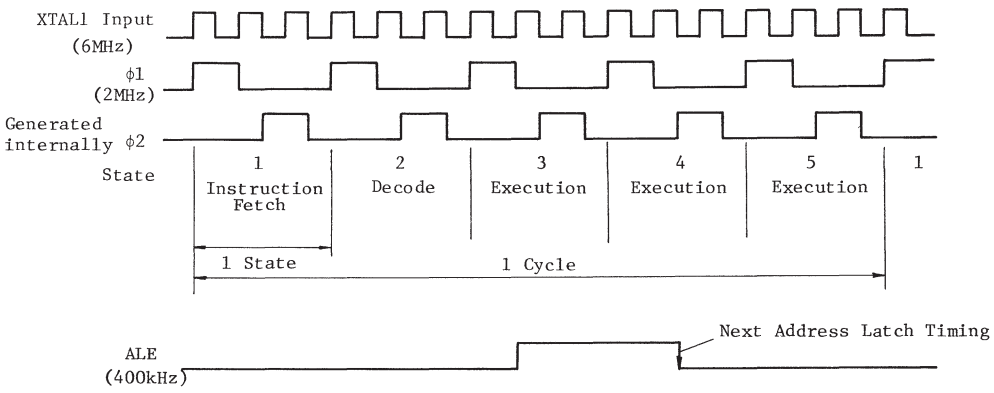


Fig.4 Instruction Cycle Timing

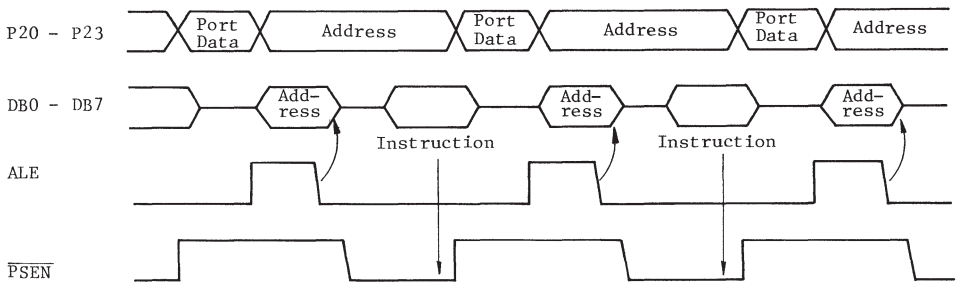
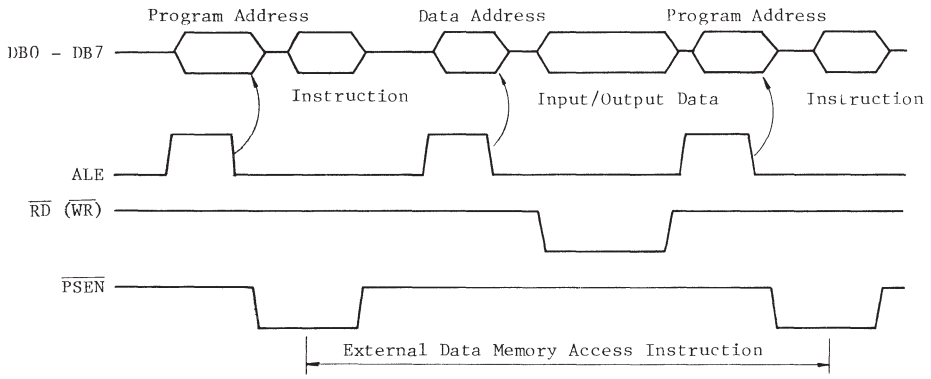


Fig.5 Timing of External Program Memory Access



Suggest we have two diagrams

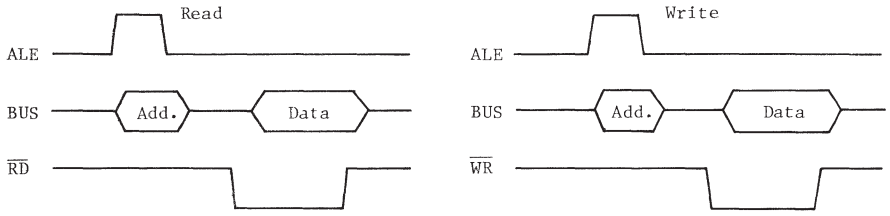


Fig.6 Timing of Accessing External Data Memory

- Figure 6 illustrates the timing of accessing the external data memory during execution of external program.

(3) Interface with I/O Expander (TMP8243P)

- The TMP8049 I/O can be easily expanded using the TMP8243 I/O Expander. This device uses only the lower half 4-bits of Port 2 for communication with the TMP8049. The TMP8243 contains four 4-bit I/O ports which serve as extensions of one chip I/O and are addressed as Ports (4-7). All communication takes place over the lower half of Port 2 (P20 - P23) with timing provided by an output pulse on the PROG pin. Each transfer consists of two 4-bit nibbles the first containing the "OP Code" and port address and the second containing the actual 4-bits of data.

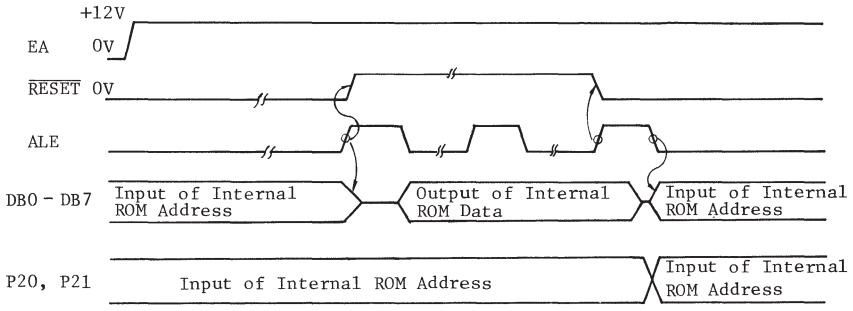


Fig.7 Timing of Rading Internal Program Memory

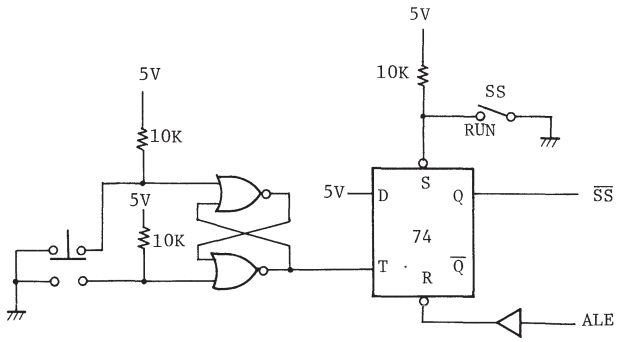


Fig.8(a) Single Step Circuit

(4) Reading of Internal Program Memory

- The processor is placed in the READ mode by applying +12V to the EA pin and 0V to the RESET pin. The address of the location to be read is then applied to BUS and the low order 2-bits of Port 2. The address is latched by a 0 to 1 transition on RESET and the high level causes the contents of program memory location addressed to appear on the eight lines of BUS.
- Figure 7 illustrates the timing diagram for this operation.

(5) Single Step Operation.

- A single step feature useful for debug can be implemented by utilizing a circuit shown in Figure 8 (a) combined with the SS pin and ALE pin.
- A D-type flip flop with set and reset is used to generate $\overline{SS}$. In the run mode $\overline{SS}$ is held high by keeping the flip flop set. To enter single step, set is removed allowing ALE to bring $\overline{SS}$ low via reset input. The next instruction is started by clocking a "1" into the FF which will not appear on $\overline{SS}$ unless ALE is high removing reset. In response to SS going high the processor begins an instruction fetch which brings ALE low resetting FF and causing the processor to again enter the stopped state.
- The timeing deagram in this case is as shown in Figure 8 (b). (EA = 5V).

(6) Lower Power Stand-by Mode.

- The TMP8049 has been organized to allow power to be removed from all but the volatile, 128 × 8 data RAM array. In power down mode the contents of data RAM can be maintained while drawing typically 10 - 15% of normal operating power requirements.

  VCC serves as the 5V supply for the bulk of the TMP8049 while the V_{DD} supplies only the RAM array. In standby mode VCC is reduced to 0V but V_{DD} is kept at 5V. Applying a low level to reset inhibits any access to the RAM by the processor and guarantees that RAM cannot be inadvertently altered as power is removed from VCC.

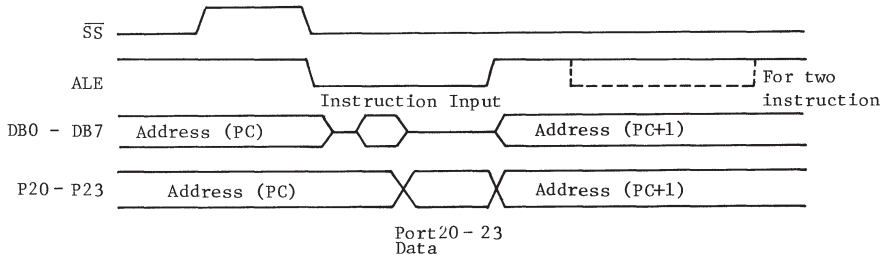


Fig.8(b) Single Step Operation Timing

INSTRUCTION

ACCUMULATOR INSTRUCTION

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
ADD A,Rr	0	1	1	0	1	r	r	r	(A)←(A)+(Rr) r = 0 - 7	1	1	○	○
ADD A,@Rr	0	1	1	0	0	0	0	r	(A)←(A)+(Rr) r = 0, 1	1	1	○	○
ADD A,#Data	0 d7	0 d6	0 d5	0 d4	0 d3	0 d2	1 d1	1 d0	(A)←(A)+Data	2	2	○	○
ADDC A,Rr	0	1	1	1	1	r	r	r	(A)←(A)+(Rr)+(C) r = 0 - 7	1	1	○	○
ADDC A,@Rr	0	1	1	1	0	0	0	r	(A)←(A)+((Rr))+(C) r = 0, 1	1	1	○	○
ADDC A,#Data	0 d7	0 d6	0 d5	1 d4	0 d3	0 d2	1 d1	1 d0	(A)←(A)+Data+(C)	2	2	○	○
ANL A,Rr	0	1	0	1	1	r	r	r	(A)←(A)∧(Rr) r = 0 - 7	1	1	-	-
ANL A,@Rr	0	1	0	1	0	0	0	r	(A)←(A)∧((Rr)) r = 0, 1	1	1	-	-
ANL A,#Data	0 d7	1 d6	0 d5	1 d4	0 d3	0 d2	1 d1	1 d0	(A)←(A)∧Data	2	2	-	-
ORL A,Rr	0	1	0	0	1	r	r	r	(A)←(A)∨(Rr) r = 0 - 7	1	1	-	-
ORL A,@Rr	0	1	0	0	0	0	0	r	(A)←(A)∨((Rr)) r = 0, 1	1	1	-	-
ORL A,#Data	0 d7	1 d6	0 d5	0 d4	0 d3	0 d2	1 d1	1 d0	(A)←(A)∨Data	2	2	-	-
XRL A,Rr	1	1	0	1	1	r	r	r	(A)←(A)∀(Rr) r = 0 - 7	1	1	-	-
XRL A,@Rr	1	1	0	1	0	0	0	r	(A)←(A)∀((Rr)) r = 0, 1	1	1	-	-
XRL A,#Data	1 d7	1 d6	0 d5	1 d4	0 d3	0 d2	1 d1	1 d0	(A)←(A)∀Data	2	2	-	-
INC A	0	0	0	1	0	1	1	1	(A)←(A)+1	1	1	-	-
DEC A	0	0	0	0	0	1	1	1	(A)←(A)-1	1	1	-	-
CLR A	0	0	1	0	0	1	1	1	(A)←0	1	1	-	-
CPL A	0	0	1	1	0	1	1	1	(A)←NOT (A)	1	1	-	-
DA A	0	1	0	1	0	1	1	1	Decimal Adjust Accumulator	1	1	○	-
SWAP A	0	1	0	0	0	1	1	1	(A4-7)⇄(A0-3)	1	1	-	-

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
RL A	1	1	1	0	0	1	1	1	(An+1)← (An) n = 0 - 6 (A0)← (A7)	1	1	-	-
RLC A	1	1	1	1	0	1	1	1	(An+1)← (An) n = 0 - 6 (C)← (A7) (A0)← (C)	1	1	-	-
RR A	0	1	1	1	0	1	1	1	(An)← (An+1) n = 0 - 6 (A7)←(A0)	1	1	-	-
RRC A	0	1	1	0	0	1	1	1	(An)← (An+1) n = 0 - 6 (C)←(A0) (A7)← (C)	1	1	-	-

Input/Output Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				A	AC
IN A,Pp	0	0	0	0	1	0	P	P	(A)← (Pp) P = 1, 2	1	2	-	-
OUTL Pp,A	0	0	1	1	1	0	P	P	(Pp)←(A) P = 1, 2	1	2	-	-
ANL Pp,#Data	1 d7	0 d6	0 d5	1 d4	1 d3	0 d2	P d1	P d0	(Pp)←(Pp)∧Data P = 1, 2	2	2	-	-
ORL Pp,#Data	1 d7	0 d6	0 d5	0 d4	1 d3	0 d2	P d1	P d0	(Pp)←(Pp)∨Data P = 1, 2	2	2	-	-
INS A,BUS	0	0	0	0	1	0	0	0	(A)←(BUS)	1	2	-	-
OUTL BUS,A	0	0	0	0	0	0	1	0	(BUS)←(A)	1	2	-	-
ANL BUS,#Data	1 d7	0 d6	0 d5	1 d4	1 d3	0 d2	0 d1	0 d0	(BUS)←(BUS)∧Data	2	2	-	-
ORL BUS,#Data	1 d7	0 d6	0 d5	0 d4	1 d3	0 d2	0 d1	0 d0	(BUS)←(BUS)∨Data	2	2	-	-
MOVD A,Pp	0	0	0	0	1	1	P	P	(A0-3)←(Pp) (A4-7)←0 P = 4 - 7	1	2	-	-
MOVD Pp,A	0	0	1	1	1	1	P	P	(Pp)←(A0-3) P = 4 - 7	1	2	-	-

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
ANLD Pp,A	1	0	0	1	1	1	P	P	(Pp)←(Pp)∧(A0-3) P = 4 - 7	1	2	-	-
ORLD Pp,A	1	0	0	0	1	1	P	P	(Pp)←(Pp)∨(A0-3) P = 4 - 7	1	2	-	-

Register Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
INC Rr	0	0	0	1	1	r	r	r	(Rr)←(Rr)+1 r = 0 - 7	1	1	-	-
INC @Rr	0	0	0	1	0	0	0	r	((Rr))←((Rr))+1 r = 0, 1	1	1	-	-
DEC Rr	1	1	0	0	1	r	r	r	(Rr)←(Rr)-1 r = 0 - 7	1	1	-	-

Branch Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
JMP Address	a10 a7	a9 a6	a8 a5	1 a4	0 a3	1 a2	0 a1	0 a0	(PC0-7)←(a0-7) (PC8-10)←(a8-10) (PC11)←DBF	2	2	-	-
JMPP @A	1	0	1	1	0	0	1	1	(PC0-7)←((A))	1	2	-	-
DJNZ Rr, Address	1 a7	1 a6	1 a5	0 a4	1 a3	r a2	r a1	r a0	(Rr)←(Rr)-1 if Rr not 0 (PC0-7)←(a0-7)	2	2	-	-
JC Address	1 a7	1 a6	1 a5	1 a4	0 a3	1 a2	1 a1	0 a0	(PC0-7)←(a0-7) if C = 1 (PC) = (PC)+2 if C = 0	2	2	-	-
JNC Address	1 a7	1 a6	1 a5	0 a4	0 a3	1 a2	1 a1	0 a0	(PC0-7)←(a0-7) if C = 0 (PC)←(PC)+2 if C = 1	2	2	-	-

Mnemonic	Instruction								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
JZ Address	1 a7	1 a6	0 a5	0 a4	0 a3	1 a2	1 a1	0 a0	(PC0-7)←(a0-7) if (A) = 0 (PC)←(PC)+2 if (A) ≠ 0	2	2	-	-
JNZ Address	1 a7	0 a6	0 a5	1 a4	0 a3	1 a2	1 a1	0 a0	(PC0-7)←(a0-7) if (A) ≠ 0 (PC)←(PC)+2 if (A) = 0	2	2	-	-
JTO Address	0 a7	0 a6	1 a5	1 a4	0 a3	1 a2	1 a1	0 a0	(PC0-7)←(a0-7) if TO = 1 (PC)←(PC)+2 if TO = 0	2	2	-	-
JNTO Address	0 a7	0 a6	1 a5	0 a4	0 a3	1 a2	1 a1	0 a0	(PC0-7)←(a0-7) if TO = 0 (PC)←(PC)+2 if TO = 1	2	2	-	-
JT1 Address	0 a7	1 a6	0 a5	1 a4	0 a3	1 a2	1 a1	0 a0	(PC0-7)←(a0-7) if T1 = 1 (PC)←(PC)+2 if T1 = 0	2	2	-	-
JNT1 Address	0 a7	1 a6	0 a5	0 a4	0 a3	1 a2	1 a1	0 a0	(PC0-7)←(a0-7) if T1 = 0 (PC)←(PC)+2 if T1 = 1	2	2	-	-
JF0 Address	1 a7	0 a6	1 a5	1 a4	0 a3	1 a2	1 a1	0 a0	(PC0-7)←(a0-7) if F0 = 1 (PC)←(PC)+2 if F0 = 0	2	2	-	-
JF1 Address	0 a7	1 a6	1 a5	1 a4	0 a3	1 a2	1 a1	0 a0	(PC0-7)←(a0-7) if F1 = 1 (PC)←(PC)+2 if F1 = 0	2	2	-	-
JTF Address	0 a7	0 a6	0 a5	1 a4	0 a3	1 a2	1 a1	0 a0	(PC0-7)←(a0-7) if TF = 1 (PC)←(PC)+2 if TF = 0	2	2	-	-
JN1 Address	1 a7	0 a6	0 a5	0 a4	0 a3	1 a2	1 a1	0 a0	(PC0-7)←(a0-7) if INT = 0 (PC)←(PC)+2 if INT = 1	2	2	-	-
JBb Address	b2 a7	b1 a6	b0 a5	1 a4	0 a3	0 a2	1 a1	0 a0	(PC0-7)←(a0-7) if Bb = 1 (PC)←(PC)+2 if Bb = 0 (b = 0 - 7)	2	2	-	-

Subroutine Instruction

Mnemonics	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
CALL Address	a10 a7	a9 a6	a8 a5	1 a4	0 a3	1 a2	0 a1	0 a0	((SP))← (PC),(PSW4-7) (SP)←(SP)+1 (PC8-10)←(a8-10) (PC0-7)←(a0-7) (PC11)←DBF	2	2	-	-
RET	1	0	0	0	0	0	1	1	(SP)←(SP)-1 (PC)←((SP))	1	2	-	-
RETR	1	0	0	1	0	0	1	1	(SP)←(SP)-1 (PC)←((SP)) (PSW4-7)←((SP))	1	2	-	-

Flag Manipulation Instruction

Mnemonics	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
CLR C	1	0	0	1	0	1	1	1	(C)←0	1	1	○	-
CPL C	1	0	1	0	0	1	1	1	(C)←NOT(C)	1	1	○	-
CLR F0	1	0	0	0	0	1	0	1	(F0)←0	1	1	-	-
CPL F0	1	0	0	1	0	1	0	1	(F0)←NOT(F0)	1	1	-	-
CLR F1	1	0	1	0	0	1	0	1	(F1)←0	1	1	-	-
CPL F1	1	0	1	1	0	1	0	1	(F1)←NOT(F1)	1	1	-	-

Data Transter Instruction

Mnemonics	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
MOV A,Rr	1	1	1	1	1	r	r	r	(A)←(Rr) r = 0 – 7	1	1	-	-
MOV A,@Rr	1	1	1	1	0	0	0	r	(A)←((Rr)) r = 0, 1	1	1	-	-
MOV A,#Data	0 d7	0 d6	1 d5	0 d4	0 d3	0 d2	1 d1	1 d0	(A)←Data	2	2	-	-
MOV Rr,A	1	0	1	0	1	r	r	r	(Rr)←(A) r = 0 – 7	1	1	-	-

Mnemonics	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
MOV @Rr,A	1	0	1	0	0	0	0	r	((Rr))←(A) r = 0, 1	1	1	-	-
MOV Rr,#Data	1 d7	0 d6	1 d5	1 d4	1 d3	r d2	r d1	r d0	(Rr)←Data r = 0 - 7	2	2	-	-
MOV @Rr,#Data	1 d7	0 d6	1 d5	1 d4	0 d3	0 d2	0 d1	r d0	((Rr))←Data r = 0, 1	2	2	-	-
MOV A,PSW	1	1	0	0	0	1	1	1	(A)←(PSW)	1	1	-	-
MOV PSW,A	1	1	0	1	0	1	1	1	(PSW)←(A)	1	1	-	-
XCH A,Rr	0	0	1	0	1	r	r	r	(A)⇄(Rr) r = 0 - 7	1	1	-	-
XCH A,@Rr	0	0	1	0	0	0	0	r	(A)⇄((Rr)) r = 0, 1	1	1	-	-
XCHD A,@Rr	0	0	1	1	0	0	0	r	(A0-3)⇄((Rr0-3)) r = 0, 1	1	1	-	-
MOVX A,@Rr	1	0	0	0	0	0	0	r	(A)←((Rr)) r = 0, 1	1	2	-	-
MOVX @Rr,A	1	0	0	1	0	0	0	r	((Rr))←(A) r = 0, 1	1	2	-	-
MOVP A,@A	1	0	1	0	0	0	1	1	(PC0-7)←(A) (A)←((PC))	1	2	-	-
MOVP3 A,@A	1	1	1	0	0	0	1	1	(PC0-7)←(A) (PC8-11)←0011 (A)←((PC))	1	2	-	-

Timer/Counter Instruction

Mnemonics	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
MOV A,T	0	1	0	0	0	0	1	0	(A)←(T)	1	1	-	-
MOV T,A	0	1	1	0	0	0	1	0	(T)←(A)	1	1	-	-
STRT T	0	1	0	1	0	1	0	1	Counting is started in the timer mode	1	1	-	-
STRT CNT	0	1	0	0	0	1	0	1	Counting is started in the event counter mode	1	1	-	-

Mnemonics	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
STOP TCNT	0	1	1	0	0	1	0	1	Stop both time accumulation and event counting	1	1	-	-
EN TCNTI	0	0	1	0	0	1	0	1	Timer interrupt is enabled	1	1	-	-
DIS TCNTI	0	0	1	1	0	1	0	1	Timer interrupt is disabled	1	1	-	-

Control Instruction

Mnemonics	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
EN I	0	0	0	0	0	1	0	1	External interrupt is enabled	1	1	-	-
DIS I	0	0	0	1	0	1	0	1	External interrupt is disabled	1	1	-	-
SEL RB0	1	1	0	0	0	1	0	1	(BS)←0	1	1	-	-
SEL RB1	1	1	0	1	0	1	0	1	(BS)←1	1	1	-	-
SEL MB0	1	1	1	0	0	1	0	1	(DBF)←0	1	1	-	-
SEL MB1	1	1	1	1	0	1	0	1	(DBF)←1	1	1	-	-
ENTO CLK	0	1	1	1	0	1	0	1	T_0 is enabled to act as the clock output	1	1	-	-
NOP	0	0	0	0	0	0	0	0	No operation	1	1	-	-

TMP8049P/8039P/8049P-6/8039P-6

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	V_{DD} Supply Voltage (with respect to GND (V_{SS}))	-0.5V to +7V
V_{CC}	V_{CC} Supply Voltage (with respect to GND (V_{SS}))	-0.5V to +7V
V_{INA}	Input Voltage (Except EA)	-0.5V to +7V
V_{INB}	Input Voltage (Only EA)	-0.5V to +13V
P_D	Power Dissipation (Ta=25°C)	1.5W
T_{SOLDER}	Soldering Temperature (Soldering Time 10 sec.)	260°C
T_{STG}	Storage Temperature	-55°C to 150°C
T_{OPR}	Operating Temperature	0°C to 70°C

DC CHARACTERISTCS

TA=0°C to 70°C, $V_{CC}=V_{DD}=+5V\pm10\%$, $V_{SS}=0V$, Unless Otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage		-0.5	-	0.8	V
V_{IH}	Input High Voltage (Except XTAL1, XTAL2, $\overline{RESET}$)		2.0	-	V_{CC}	V
V_{IH1}	Input High Voltage (XTAL1, XTAL2, $\overline{RESET}$)		3.8	-	V_{CC}	V
V_{OL}	Output Low Voltage (BUS)	I_{OL}=2.0mA	-	-	0.45	V
V_{OL1}	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	I_{OL}=1.8mA	-	-	0.45	V
V_{OL2}	Output Low Voltage (PROG)	I_{OL}=1.0mA	-	-	0.45	V
V_{OL3}	Output Low Voltage (For other output pins)	I_{OL}=1.6mA	-	-	0.45	V
V_{OH}	Output High Voltage (BUS)	I_{OH}=-400μA	2.4	-	-	V
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	I_{OH}=-100μA	2.4	-	-	V
V_{OH2}	Output High Voltage (For tothe output pins)	I_{OH}=-40μA	2.4	-	-	V
I_{LI}	Input Leak Current (T1, $\overline{INT}$)	$V_{SS}\leqq V_{IN}\leqq V_{CC}$	-	-	±10	μA
I_{LI1}	Input Leak Current (P10-17, P20-P27, EA, $\overline{SS}$)	$V_{SS}+0.45\leqq V_{IN}\leqq V_{CC}$	-	-	-500	μA
I_{LO}	Output Leak Current (BUS, TO) (High impedance condition)	$V_{SS}+0.45\leqq V_{IN}\leqq V_{CC}$	-	-	±10	μA
I_{DD}	V_{DD} Supply Current		-	-	50	mA
$I_{DD}+I_{CC}$	Total Supply Current		-	-	170	mA

AC CHARACTERISTICS

TA=0°C to 70°C, $V_{CC}=V_{DD}=+5V\pm10\%$, $V_{SS}=0V$, Unless Otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITION	TMP8049P/ TMP8039P		TMP8049P-6/ TMP8039P-6		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{LL}	ALE Pulse Width		150	-	400	-	ns
t_{AL}	Address Setup Time (ALE)		70	-	150	-	ns
t_{LA}	Address Hold Time (ALE)		50	-	80	-	ns
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)		300	-	700	-	ns
t_{DW}	Data Setup Time ($\overline{WR}$)		250	-	500	-	ns
t_{WD}	Data Hold Time ($\overline{WR}$)	C_L=20pF	40	-	120	-	ns
t_{CY}	Cycle Time	11MHz XTAL (6MHz XTAL for -6)	1.36	15.0	2.5	15.0	μs
t_{DR}	Data Hold Time ($\overline{PSEN}$, $\overline{RD}$)		0	100	0	200	ns
t_{RD}	Data Input Read Time ($\overline{PSEN}$, $\overline{RD}$)		-	200	-	500	ns
t_{AW}	Address Setup Time ($\overline{WR}$)		200	-	230	-	ns
t_{AD}	Address Setup Time (Data Input)		-	400	-	950	ns
t_{AFC}	Address Float Time ($\overline{RD}$, $\overline{PSEN}$)		-10	-	0	-	ns
t_{CP}	Port Control Setup Time (PROG)		100	-	110	-	ns
t_{PC}	Port Control Hold Time (PROG)		60	-	130	-	ns
t_{PR}	Port 2 Input Data Set Time (PROG)		-	650	-	810	ns
t_{DP}	Output Data Setup Time (PROG)		200	-	220	-	ns
t_{PD}	Output Data Hold Time (PROG)		20	-	65	-	ns
t_{PF}	Port 2 Input Data Hold Time (PROG)		0	150	0	150	ns
t_{PP}	PROG Pulse Width		700	-	1510	-	ns
t_{PL}	Port 2 I/O Data Setup Time		250	-	500	-	ns
t_{LP}	Port 2 I/O Data Hold Time		120	-	150	-	ns

Control Outputs : C_L=80pF, BUS Outputs : C_L=150pF

TMP8049PI-6/8039PI-6 : INDUSTRIAL SPECIFICATION.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	V_{DD} Supply Voltage (with respect to GND (V_{SS}))	-0.5V to +7V
V_{CC}	V_{CC} Supply Voltage (with respect ro GND (V_{SS}))	-0.5V to +7V
V_{INA}	Input Voltage (Except EA)	-0.5V to +7V
V_{INB}	Input Voltage (Only EA)	-0.5V to +13V
P_D	Power Dissipation (Ta=25°C)	1.5W
T_{SOLDER}	Soldering Temperature (Soldering Time 10 sec.)	260°C
T_{STG}	Storage Temperature	-55°C to 150°C
T_{OPR}	Operating Temperature	-40°C to 85°C

DC CHARACTERISTICS TA=-40°C to 85°C, $V_{CC}=V_{DD}=+5V\pm10\%$, $V_{SS}=0V$, Unless Otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage		-0.5	-	0.6	V
V_{IH}	Input High Voltage (Except XTAL1, XTAL2, $\overline{RESET}$)		2.2	-	V_{CC}	V
V_{IH1}	Input High Voltage (XTAL1, XTAL2, $\overline{RESET}$)		3.8	-	V_{CC}	V
V_{OL}	Output Low Voltage (BUS)	I_{OL}=1.6mA	-	-	0.45	V
V_{OL1}	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	I_{OL}=1.6mA	-	-	0.45	V
V_{OL2}	Output Low Voltage (PROG)	I_{OL}=0.8mA	-	-	0.45	V
V_{OL3}	Output Low Voltage (For other output pins)	I_{OL}=1.2mA	-	-	0.45	V
V_{OH}	Output High Voltage (BUS)	I_{OH}=-80μA	2.4	-	-	V
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	I_{OH}=-80μA	2.4	-	-	V
V_{OH2}	Output High Voltage (For other output pins)	I_{OH}=-30μA	2.4	-	-	V
I_{LI}	Input Leak Current (T1, $\overline{INT}$)	$V_{SS}\leq V_{IN}\leq V_{CC}$	-	-	±10	μA
I_{LI1}	Input Leak Current (P10-17, P20-P27, EA, $\overline{SS}$)	$V_{SS}+0.45\leq V_{IN}\leq V_{CC}$	-	-	-700	μA
I_{LO}	Output Leak Current (BUS, TO) (High impedance condition)	$V_{SS}+0.45\leq V_{IN}\leq V_{CC}$	-	-	±10	μA
I_{DD}	V_{DD} Supply Current		-	-	50	mA
$I_{DD}+I_{CC}$	Total Supply Current		-	-	170	mA

AC CHARACTERISTICS

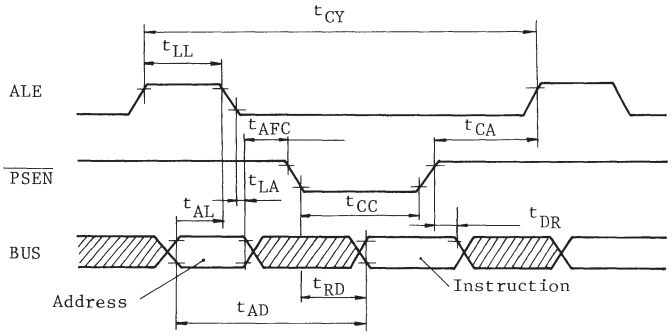
T_A=-40°C to 85°C, $V_{CC}=V_{DD}$=+5V±10%, V_{SS}=0V, Unless otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{LL}	ALE Pulse Width		200	-	-	ns
t_{AL}	Address Setup Time (ALE)		120	-	-	ns
t_{LA}	Address Hold Time (ALE)		80	-	-	ns
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)		400	-	-	ns
t_{DW}	Data Setup Time ($\overline{WR}$)		420	-	-	ns
t_{WD}	Data Hold Time ($\overline{WR}$)	C_L=20pF	80	-	-	ns
t_{CY}	Cycle Time		2.5	-	15.0	μs
t_{DR}	Data Hold Time ($\overline{PSEN}$, $\overline{RD}$)		0	-	200	ns
t_{RD}	Data Input Read Time ($\overline{PSEN}$, $\overline{RD}$)		-	-	400	ns
t_{AW}	Address Setup Time ($\overline{WR}$)		230	-	-	ns
t_{AD}	Address Setup Time (Data Input)		-	-	600	ns
t_{AFC}	Address Float Time ($\overline{RD}$, $\overline{PSEN}$)		-40	-	-	ns
t_{CA}	Internal between Control Pulse and ALE		10	-	-	ns
t_{CP}	Port Control Setup Time (PROG)		115	-	-	ns
t_{PC}	Port Control Hold Time (PROG)		65	-	-	ns
t_{PR}	Port 2 Input Data Set Time (PROG)		-	-	860	ns
t_{DP}	Output Data Setup Time (PROG)		230	-	-	ns
t_{PD}	Output Data Hold Time (PROG)		25	-	-	ns
t_{PF}	Port2 Input Data Hold Time (PROG)		0	-	160	ns
t_{PP}	PROG Pulse Width		920	-	-	ns
t_{PL}	Port 2 I/O Data Setup Time		300	-	-	ns
t_{LP}	Port 2 I/O Data Hold Time		120	-	-	ns

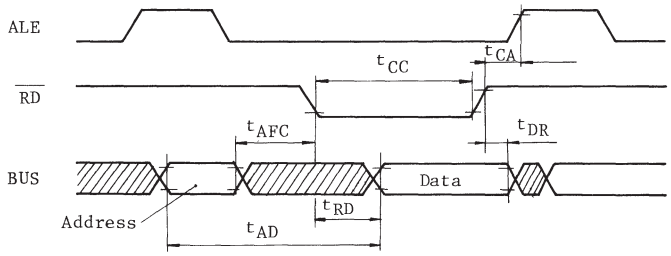
Note : tcy=2.5μs, Control Output: C_L=80pF, BUS Output: C_L=150pF, PORT 20-23: C_L=80pF.

TIMING WAVEFORM

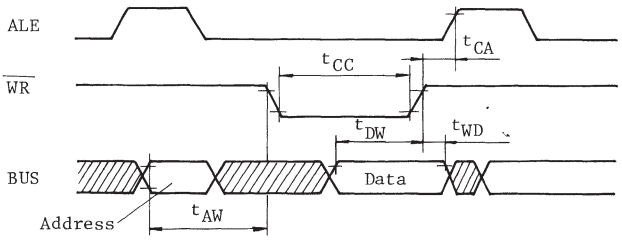
A. Instruction Fetch from External Program Memory



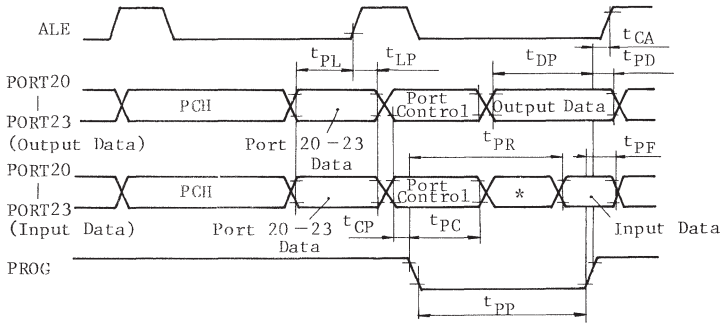
B. Read from External Data Memory



C. Write into External Data Memory



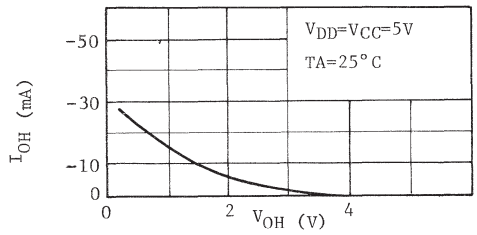
D. Timing of Port 2 during Expander Instruction Execution



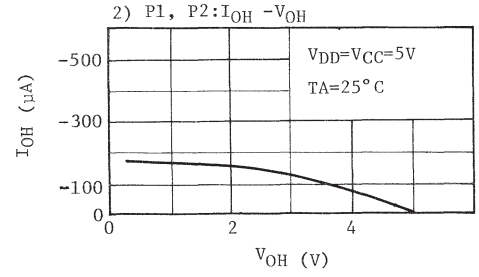
* Input Enabled State

TYPICAL CHARACTERISTICS

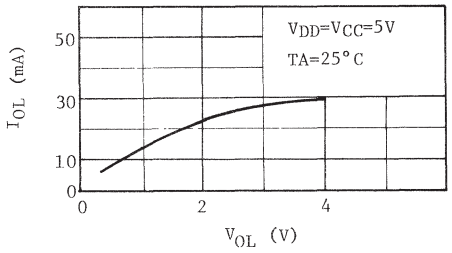
1) BUS: I_{OH} - V_{OH}



2) P1, P2: I_{OH} - V_{OH}



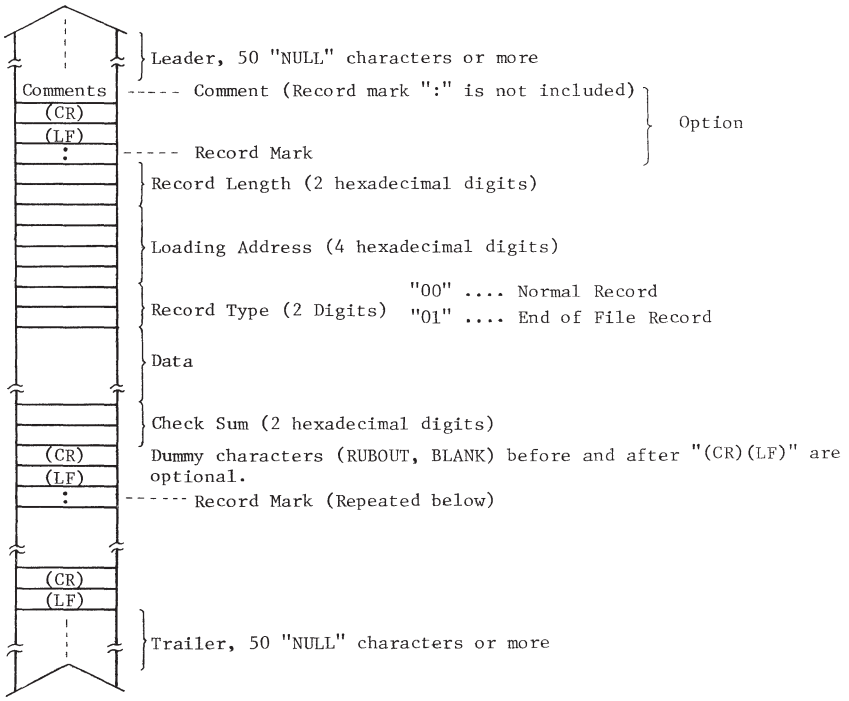
3) BUS, P1, P2: I_{OL} - V_{OL}



PROGRAM TAPE FORMAT

TMP8049 programs are delivered in the form of paper tape with the following format and it is required to attach the tape list. The format of paper tape is same as the Intel type object tape (hexadecimal tape output by Intel MDS system, PROMPT 48 Development Tool, etc.)

(1) Tape Format

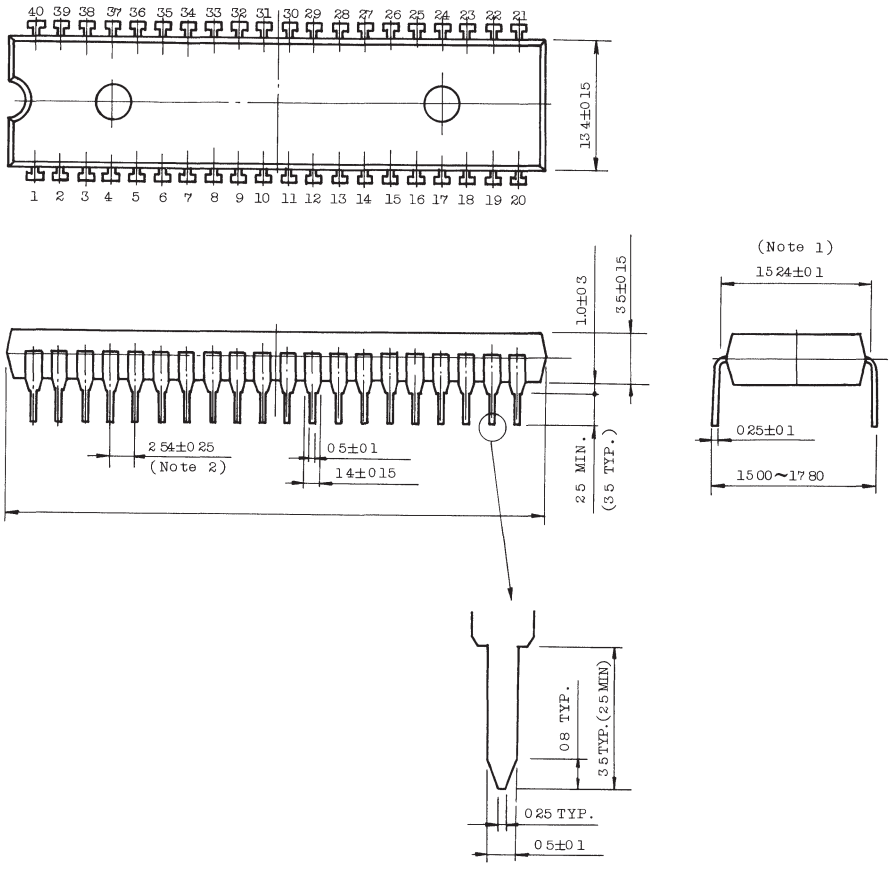


(2) Example of Tape List

```
TOSHIBA MICRO COMPUTER TLCS-84
:100000000665C7D79CF50F3F951FED55A8FF16E570
:1000100088884DDE67D31F5D8ABA6DF292F113F5C1
:100020004FF1FB5DFFDAA96A99CF7DF94A346B7C09
:10003000197352F729F12F79AA9C057C5B851EED77
                    :
                    :
:1003C0005DFDB5E556A67277F61A51C631CF9F0E80
:1003D000BD2F6F20E8BB1977E3FB5AD1F41FDAA7E2
:1003E000B53D42E0EC32546025B7308CDD52063D1D
:1003F000B4BE9E9E345B6138060B20VC372BF60BD6
:00000001FF
```

OUTLINE DRAWING

Unit in mm



Note: 1. This dimension is measured at the center of bending point of leads.

2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.